MICROLOGIC® SHIFT-COUNTER INTEGRATED CIRCUITS

by George Powers

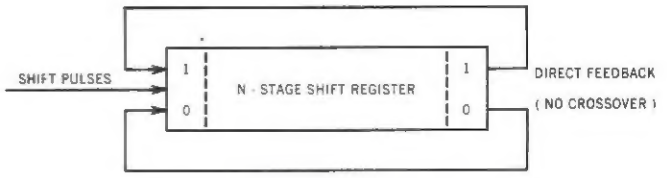
I. INTRODUCTION

Since the original publication of this article in 1963, the cost of integrated circuits has plummeted, while the complexity of microelectronic devices has doubled, and doubled again. Therefore, many of the comparisons drawn earlier do not hold today. In fact, some of the counters that were described as reasonable alternatives only two years ago have a rather quaint appearance when compared with the designs which are now possible with today's versatile flip-flops. Nevertheless, the shift-register technique is still attractive from several viewpoints, and it certainly does not sacrifice economy.

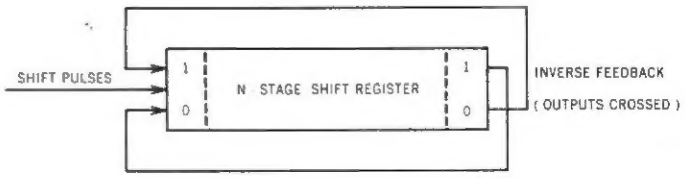
The application of the Micrologic® half shift-register IC's to shift-counters is omitted altogether, since the current emphasis is on μL J-K flip-flops or DTμL clocked flip-flops. In few instances will half shift-registers produce a more economical solution. Other counting techniques (several binary types) have been omitted in this revision, since the basis for economic comparison no longer exists. The interested reader can obtain information on alternative approaches in any one of the articles listed under References.

II. DESCRIPTION

The counters under discussion are the simplest non-binary counters extant. They consist of an N-stage shift register closed upon itself to form a ring. In fact, "ring counter" would be an appropriate description of the circuit except that this name has been preempted by a similar, yet quite different, counter circuit. The fundamental difference between the two is that the latter has a modulus* of N, while the subject of this discussion may have a modulus of either 2N or 2N-1 (see Fig. 1). The ring counter closes on itself directly; the shift-counter closes with a cross-over that feeds back the complement of the output. In general, the shift-counter is self-starting, needing a minimum of additional circuitry to effect and maintain the proper operating mode, whereas the ring counter is difficult to operate properly. The shift counter is more economical than flip-flops, which are still the most expensive single integrated logic devices. But, unlike ring counters, discrete counts must be decoded, requiring more gate circuits. However, the cost trade-off favors gates.



(a) RING COUNTER (MODULUS = N)



(b) SHIFT COUNTER (MODULUS = 2N)

FIG. 1. Counters based on shift registers.

*Modulus—A real, positive quantity that expresses the measure of some function; in this case, it is the number of counts per cycle. (Plural is moduli, adjective form is modulo.)

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The Modulo-10 Shift Counter

The modulo-10 counter appears so frequently in practical applications that it will be used as an illustrative example. In Fig. 2, the general block diagram of Fig. 1 is interpreted with μL 923 or μL 926 J-K flip-flops. Five stages are employed since $2N = 10$ — the required modulus. The desired sequence of operation is given in Fig. 3. Note that the waveforms shown are logic waveforms, not electrical waveforms. A solid portion indicates a logic one signal; a blank portion indicates a logic zero signal. This notation has the virtue of showing the relative timing of a logic system without committing the design to any particular circuit type. For the RTL circuits of Fig. 2, the solid portion is interpreted as a low signal from the one output, while the blank portions are high signals from the same output terminal. If the counter were constructed of DTL flip-flops such as the DTμL 945/948, the opposite sense would apply—solid portions indicating a high signal, blank portions a low signal. In either case, the logical timing diagram of Fig. 3 would suffice.

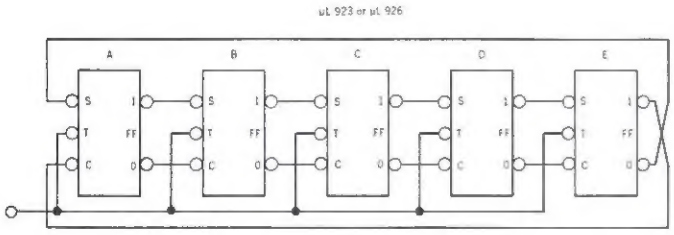


FIG. 2. Modulo-10 shift counter.

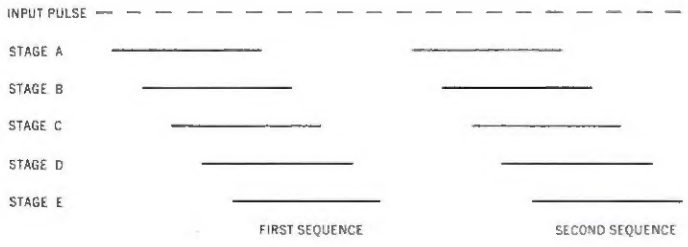


FIG. 3. Modulo-10 shift counter timing diagram.

Secondary Operating Modes

The total number of distinct states which a set of five binary objects may assume is given by:

$$\sum_{N=0}^{5} \binom{5}{N} = 1 + 5 + 10 + 10 + 5 + 1 = 32$$

Since only 10 of the possible 32 states are wanted, what happens when one of the unassigned states is accidentally entered? (This could occur when the circuit is initially energized or subjected to a burst of electrical noise greater than the rejection level.) The results of an analysis of these possibilities are tabulated in Fig. 4. Four modes of operation exist. The 32 states fall into three groups of 10 and one group of 2. Each of these is a closed sequence that will persist as long as there is no external disturbance. Obviously, mode 4 cannot be allowed in a modulo-10 counter, and mode 1 is preferred over modes 2 and 3 for the reasons stated in the next section. Consequently, the secondary modes must be suppressed. Figure 5 shows the method for accomplishing this function.

MODE 1

Count No.	Stage					Binary
	A	B	C	D	E	
0	0	0	0	0	0	0
1	1	0	0	0	0	16
2	1	1	0	0	0	24
3	1	1	1	0	0	28
4	1	1	1	1	0	30
5	1	1	1	1	1	31
6	0	1	1	1	1	15
7	0	0	1	1	1	7
8	0	0	0	1	1	3
9	0	0	0	0	1	1

MODE 2

Count No.	Stage					Binary
	A	B	C	D	E	
0	0	1	0	0	0	8
1	1	0	1	0	0	20
2	1	1	0	1	0	26
3	1	1	1	0	1	29
4	0	1	1	1	0	14
5	1	0	1	1	1	23
6	0	1	0	1	1	11
7	0	0	1	0	1	5
8	0	0	0	1	0	2
9	1	0	0	0	1	17

MODE 3

Count No.	Stage					Binary
	A	B	C	D	E	
0	0	0	1	0	0	4
1	1	0	0	1	0	18
2	1	1	0	0	1	25
3	0	1	1	0	0	12
4	1	0	1	1	0	22
5	1	1	0	1	1	27
6	0	1	1	0	1	13
7	0	0	1	1	0	6
8	1	0	0	1	1	19
9	0	1	0	0	1	9

MODE 4

Count No.	Stage					Binary
	A	B	C	D	E	
0	0	1	0	1	0	10
1	1	0	1	0	1	21

FIG. 4. Operating modes of a Modulo-10 counter.

An examination of the tables in Fig. 4 reveals that when the clear signal for stage A depends upon a one in stage D as well as stage E, only mode 1 is unaffected. In each of the other modes, the sequence is altered. For example, at count 3 of mode 2, the clear signal is inhibited and the counter assumes count 4 of mode 1; count 9 of mode 2 becomes count 2 of mode 1; and count 3 of mode 3 becomes count 3 of mode 1. Thus, modes 2 and 3 revert directly to mode 1. Count 1 of mode 4, however, leads into mode 2 at count 2, and thereafter to mode 1. The addition of the extra circuits assures that mode 1 will predominate under all circumstances. The additional gates can be omitted when flip-flops such as the DTμL clocked flip-flops are employed, through use of the AND gate built into the flip-flop inputs. With these devices, stage D and stage E connect to the two clear inputs accomplishing the same function without supplemental gating.

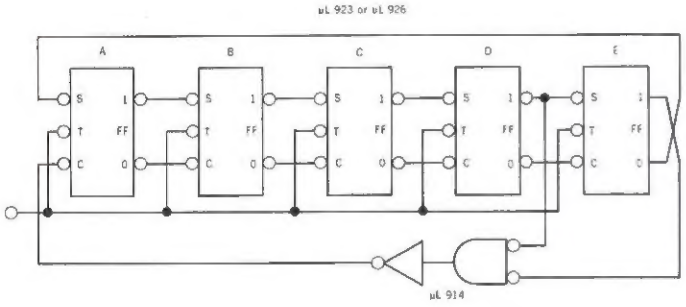


FIG. 5. Secondary mode suppression.

Decoding

One of the most beneficial characteristics of shift-counters is the simplicity of decoding individual counts. The count sequences of modes 1, 2, and 3 appear in the Karnaugh maps of Fig. 6. The simplest Boolean expression for each count in each mode is given below the maps. In all cases, there is the assumption that states which are not included in a particular sequence cannot occur, and hence, may be assigned any value that will minimize the expressions for the states which do occur.

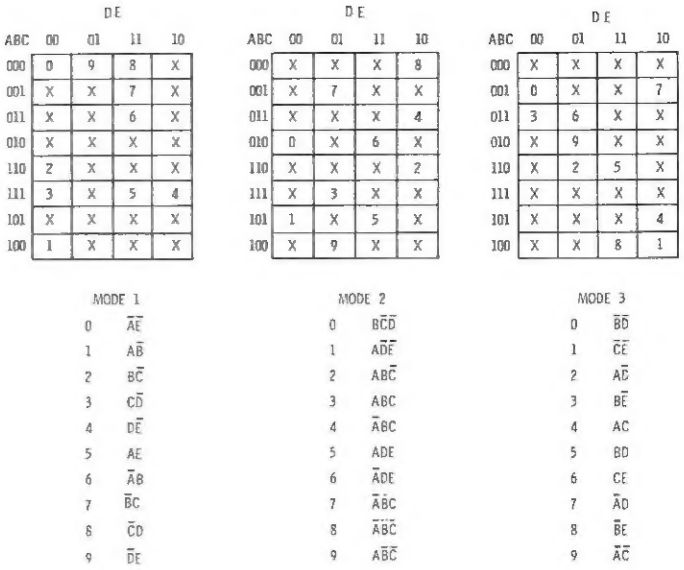


FIG. 6. Modulo-10 decoding.

It is readily apparent, from a decoding viewpoint, that mode 2 is less efficient than either of the other decimal modes. The simplest mode 2 decoding requires three-input gates, whereas modes 1 and 3 can be decoded with two-input gates. The decoding for modes 1 and 3 has the additional attribute of loading all stage outputs uniformly. There is a smaller chance of introducing "spikes" in the decoded outputs when all decoder input signals are similar in transient response.

Mode 1 is superior to mode 3 because of the waveshapes which are generated. Each stage output of a mode 1 counter is a square wave at a frequency of $1/2$ N times the input frequency. Hence, a stage output can be used directly when the application of the counter is simple frequency division. This is not the case with mode 3. At least one gate is necessary to recover the actual division ratio.

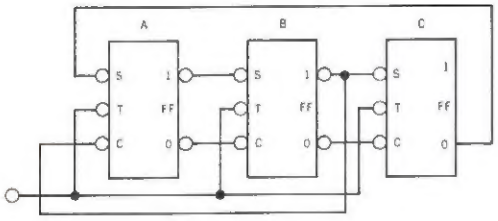
Another feature of mode 1, which may be of use in special applications, is that all stage outputs are identical, each being subjected to a phase delay equal to one period of the input signal. Thus, a shift-counter could be the basis of a multiphase clock generator.

A mode analogous to mode 1 exists for any other modulus. The technique used to assure mode 1 operation for modulo-10 counting also works for any other modulus. It is not known whether a simple way of assuring any other mode exists. If one does exist, it is probably unique and applies only to that particular modulus.

Diminished Modulus Shift-Counters

The natural modulus of a shift-counter—2N—puts all even moduli in the scope of this approach. Odd moduli can also be realized by a simple modification of the basic shift-counter. The natural modulus of 2N is diminished by skipping one count of the normal sequence. Any one of the normal counts could be skipped, but only the all-zero or all-one counts affect all stage waveshapes equally. Since the all-zero count is often selected as a reference point, the all-one count will be skipped in the examples which follow.

A useful modulus is five. Figure 7 illustrates a modulo-5 shift-counter. The only difference between the modulo-5 counter and the modulo-6 counter from which it was derived is that the feedback to the clear input of the first stage is taken from the one output of the next to last stage rather than the last stage. It is apparent that this modification produces a clear signal one count earlier than normal. In fact, the clear signal appears while the set signal from the last stage is still present. This conflict is resolved by the J-K property of the flip-flops. When both inputs are ones, the flip-flop complements. During the same interval that the last stage is set, the first stage is cleared, so that the all-one state can never exist.



A	B	C
0	0	0
1	0	0
1	1	0
0	1	1
0	0	1

FIG. 7. Modulo-5 shift counter.

The same modification—relocation of the clear feedback connection at the next to last stage — holds for all odd moduli. In the cases of 3, 5, and 7, secondary modes do not exist; but for greater moduli, sequence protection must be incorporated. The scheme used for even-modulus counters works for odd moduli as well. However, the outputs used to provide the clear signal are both displaced one stage toward the first counter stage in the process of skipping the all-one count.

III. CONCLUSION

One of the advantages ascribed to shift-counters in comparison with binary counters is a theoretically greater operating speed. This argument is based upon the fact that no stage in a shift-counter must operate any faster than 1/N times the input frequency. On the other hand, the first stage of a binary counter must operate at the input frequency. Perhaps with discrete circuits it is possible to benefit from this fact. However, the limiting speed of integrated flip-flops is solely a function of signal propagation delay. It, therefore, makes little difference whether a stage is operated as a binary or as a shift register—the problems remain the same. It is possible that the interstage wiring of a shift register can, in extreme cases, reduce the reliable shifting rate.

A difference in operating speed is evident when non-binary moduli are required. A counter based upon a modified binary scheme must necessarily use gates to achieve the desired nonbinary modulus. The delay due to these additional gates usually results in slower operation than can be realized with a shift-counter.

Two input gates are adequate for decoding shift-counters of any size. For Binary Counters, two input gates suffice only up to a count of 3. It is therefore quite feasible to use a greater number of flip-flops to reduce the number of gate packages in use. This tradeoff is quite significant when using diode-transistor Micrologic® integrated circuits due to the availability of four two-input gates in a single package. The designer is well advised to consider the possibilities offered by shift-counters.

IV. REFERENCES

1. G. Powers, "Diode-Transistor Micrologic," Fairchild APP-107, May 1965.

2. D. Davies, R. Seeds, and S. Shou, "An Integrated Charge-Control J-K Flip-Flop," IEEE Transactions On Electronic Devices, Vol. ED-11, No. 12, December 1964.